Title: NROM MEMORY DEVICE WITH HIGH-PERMITTIVITY GATE DIELECTRIC FORMED BY THE LOW TEMPERATURE OXIDIZATION OF METALS

REMARKS

Claim Rejections Under 35 U.S.C. § 112

Claim 6 was rejected under 35 U.S.C. §112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention. Claim 6 has been amended to more clearly claim the subject matter that the Applicant regards as the invention. Support for these amendments is taught in the present specification at paragraph 0046. Therefore, no new matter has been added by these amendments.

Claim Rejections Under 35 U.S.C. § 103

Claims 1, 2 and 5 were rejected under 35 U.S.C. § 103(a) as being unpatentable over Sugizaki in view of Yu (U.S. Patent No. 6,495,437). Claim 4 was rejected under 35 U.S.C. § 103(a) as being unpatentable over Sugizaki and Yu in view of Akatsu (U.S. Patent No. 5,717,635). Applicant respectfully traverses this rejection.

Sugizaki discloses a flash memory using a high-k charge trapping layer. Sugizaki neither teaches nor suggests Applicant's final structure that results from a low temperature oxidation of Al. Sugizaki uses chemical vapor deposition to form the aluminum layer. It is well known in the art that the oxidized Al results in a more uniform structure than is achievable by CVD. Additionally, it is taught by the present specification (see paragraph 0046) that this structure formed by low temperature oxidation also results in a higher tunnel barrier on the interface between the oxidized metal layer and the top insulator than between the oxidized metal layer and the tunnel insulator. Paragraph 0046 discusses the excess Al ions that have not been oxidized and the interface between these Al ions and the oxidized Al (Al₂O₃) but one skilled in the art will know that this applies to the currently claimed structure. Further, paragraph 0053 of the present specification discusses the electrical differences that result from using low temperature oxidation versus CVD as used in Sugizaki.

There is no motivation to combine Yu with Sugizaki as suggested by the Examiner. There is no stated or suggested need in Sugizaki for a more uniform thickness of the tunnel dielectric as provided by Yu. Additionally, even if it were obvious to combine Yu with Sugizaki, and Applicant maintains that it is not, the combination still would not anticipate the present invention as claimed. Yu teaches that layer 35 can be an aluminum layer that is oxidized into an aluminum oxide layer 34. However, layer 34 of Yu that is formed by oxidation is the tunnel dielectric layer

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and not the oxidized charge trapping layer as claimed in the present claims. These are obviously two completely different layers with different functions.

Akatsu teaches NOR and NAND EEPROMs. For the above reasons, even if it were obvious to combine Akatsu with Sugizaki/Yu, and Applicant maintains that it is not, the combination still would not anticipate the present invention as claimed.

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CONCLUSION

In view of the above remarks, Applicant believes that all pending claims are in condition for allowance and respectfully requests a Notice of Allowance be issued in this case. Please charge any further fees deemed necessary or credit any overpayment to Deposit Account No. 501373.

If the Examiner has any questions or concerns regarding this application, please contact the undersigned at (612) 312-2211.

Respectfully submitted,

TI Bol

Date: 7/6/06

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